Specification

400-9809-09 Version 1.1 7/31/02

1 Features

- **320 x 256 Pixels**
- **30µm Pixel Pitch**
- **Snapshot Mode Integration**
- **P-on-N or N-on-P Input Polarity**
- **Integration Capacitor Selectable**
- **3.5 and 0.17 Million e^- Well Capacity Options**
- **Adjustable Integration Time > 0.5µs**
- **Low Noise CTIA Input Circuit (300K)**
  - < 70e^-_{RMS} (default mode -high gain-)
  - < 700e^-_{RMS} (low gain)
- **Skimming (Offset Suppression)**
- **Integrate-While-Read and Integrate-Then-Read Timing**
- **Selectable Bandwidth for Optimal Noise Performance**
- **Selectable 1, 2 or 4 Outputs (2.8V Analog)**
- **Dynamic Windowing Readout**
- **Dynamic Image Transposition**
  - Image Invert [top-to-bottom]
  - Image Revert [left-to-right]
- **Extensive Built-In-Test Capability**
- **Simple Interface Requires 3 System Clocks**
- **Two Operational Mode**
  - Simple 'hands-off' Default Mode
  - User Configurable Command Mode
- **Power dissipation < 90mW (single output)**
- **Buffered Output Temperature Sensor**
- **Tested Wafers w/ Wafer Map and Die Data**
- **Low Background applications**

2 Product Description

The ISC9809 is a high performance, 320 x 256 pixel, readout integrated circuit (ROIC) for infrared detectors with snapshot mode integration. This state-of-the-art ROIC is suitable for use with p-on-n or n-on-p detector materials such as indium antimonide (InSb), mercury cadnium telluride (MCT), quantum well infrared photo diodes (QWIPs) and indium gallium arsendide (InGaAs). The ISC9809 is especially adapted for very low background conditions to support night glow and day time operation.

A simplified 'hands-off' Default Mode directly supports single output NTSC or PAL operation. Using the Command Mode, the ISC9809 supports advanced features including; dynamic image transposition, dynamic windowing, multiple output configurations, and signal 'skimming'. Both modes support integration time and gain adjustment.

Using four outputs, frame rates up to 346 frames per second can be achieved for full 320 x 256 frames. One output allows full frame rate of 110Hz. A convenient buffered temperature sensor output is available for monitoring of the ROIC substrate temperature.

The ISC9809 is fabricated using an advanced 0.6µm double poly, triple metal process which utilizes high speed CMOS transistors. High speed, precision analog circuits are combined with high density digital logic circuits to achieve this advanced featured ROIC. The ISC9809 is delivered in wafer form and is specified for operation from 80 K to 300 K.

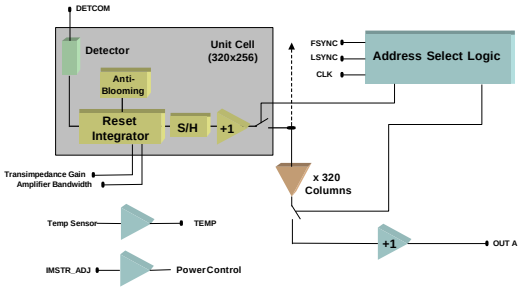


Figure 1: ISC9809 readout architecture

Figure 1 shows the block diagram for the Default Mode operation. The detector bias voltage is adjustable using the VDETCOM pad. A capacitive transimpedance amplifier input circuit (CTIA) provides a low noise front end including an anti-blooming transistor. The input CTIA has 2 selectable integration capacitors handling a charge capacity range of 0.17 and 3.5 million electrons.

The output from each unit cell is addressed to a column bus and sampled onto a column amplifier. The column amplifier is multiplexed to a one, two or four output channels. A skimming function is also provided to globally offset the output signal for high leakage current detectors such as QWIPs.

The ISC9809 pad definition is shown in Figure 2.

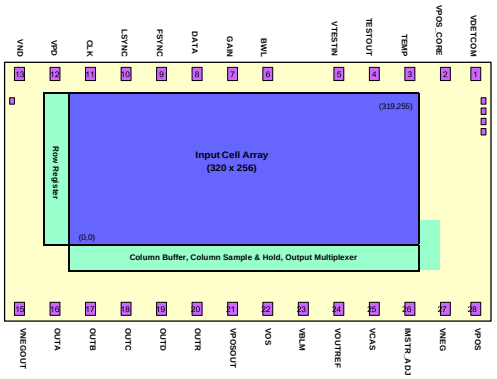


Figure 2: ISC9809 Pad Placement

3 Specifications

Maximum Ratings				
Parameter	**With Respect To**	**Min.**	**Max.**	**Units**
VPOS,VPD,VPOSOUT	VNEG,VND,VNEGOUT	-0.5 [2]	5.7 [1]	Volts
Clock Inputs	VNEG,VND,VNEGOUT	-0.5 [2]	VPD + 0.2 [1]	Volts
Outputs	VNEG,VND,VNEGOUT	0.0 [2]	VPOS	Volts
Operating Temperature		77 [2]	310 [2]	K
Storage Temperature		49 [2]	420 [2]	K

NOTES:
1. Stresses above the value listed may cause permanent damage to the device.
2. Stresses beyond the listed range may cause permanent damage to the device. This is a stress rating *only*. Functional operation of the device at these or other conditions above those indicated in the operational sections of this specification are not implied. Exposure to maximum ratings for extended periods of time may affect device reliability.

Mechanical Specifications				
Parameter	**Test Level**	**Typ.**	**Max.**	**Units**
Wafer Size	V	5		Inch
Total Die per Wafer [1]	V	72		Die/wafer
Detector Columns	IV	320		Active unit cells
Detector Rows	IV	256		Active unit cells
Detector Row and Column Pitch	IV	30		µm
Die Size [2]	IV	11.35 x 10.65		mm
Scribe Lanes in X and Y	IV	200		µm

NOTES:
1. Including all die grades
2. As measured to edge of scribe lane

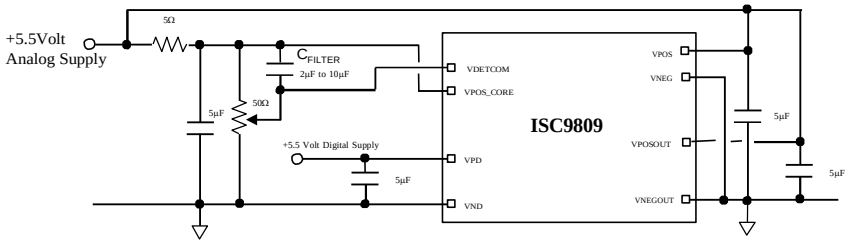
EXPLANATION OF TEST LEVELS
Test Level
I – 100% production tested.
II – 100% production tested at room temperature.
III – Sample tested only.
IV – Parameter is guaranteed by design and/or characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at room temperature.

DC Specifications (250K operation unless noted)	**Test Level**	**Min.**	**Typ.**	**Max.**	**Units**
Detector Type	IV		P-on-N or N-on-P		
Detector Impedance	IV				
RoAd	V		$> 10^7$		$\Omega.cm^2$
Cdet @ 0.5 V reverse bias	V		≤ 0.1		pF
Input Clock Rate	IV		≤ 5		MHz
Readout Noise [1]					
Maximum Gain [1]	III		≤ 70		e^-_{RMS}
Minimum Gain [2]	III		≤ 700		e^-_{RMS}
Integration Capacitor Charge Capacity					
C_{int} = 10f F @2.7 V	IV		0.17 million		e^-
C_{int} =210fF @ 2.7 V	IV		3.5 million		e^-
Transimpedance Non-Linearity [3]	IV		< ±0.5%		
Input Clock Rise and Fall	IV		10	20	nsec
Number of Outputs	IV		1, 2 or 4		
Output Interface					
R_{load}			> 500k		ohms
C_{load}			< 25		pF
Output Settling	IV		≤ 0.1% in ≤50 nsec		
Output Voltage Swing	VI	> 2.0	2.7		Volts
Output Voltage Low	V		1.6		Volts
Output Voltage High	V		4.3		Volts
Output linearity	III		±0.5%		
Max. Full Window Frame Rate [4]					
4 outputs	IV		346	346	Frames/sec
2 outputs	IV		200	201	Frames/sec
1 output	IV		100	110	Frames/sec
Power Dissipation					
Four outputs (maximum frame rate)	IV		< 150	< 175	mW
Single output (NTSC or PAL)	VI		< 90	< 100	mW

1. RoAd =$10^7\Omega*cm^2$, C_{det}=0.1pF, Tint=16msec, Gain Bit = 0 (C_{int}=10fF), Vbias = -0.5V
2. RoAd =$10^7\Omega*cm^2$, C_{det}=0.1pF, Tint=16msec, Gain Bit = 1, (C_{int}=210fF), Vbias = -0.5V
3. From least squares line fit (10% to 90% of the signal dynamic range)
4. C_{load} =25pF max., R_{load}=500kΩ min

DC Specifications (cont.)	**Voltage** (volts)	**Current** (mA)	**Peak Current** (mA)	**Max. Ext. Resistance** (Ω)	**Gain to Output**
Bias Voltages (highest power)					
VPOS	5.5	< 5	< 25	5	< 0.3
VNEG	0	< 15	< 20	2	< 0.2
VPD	5.5	< 1	< 20	10	< 0.1
VND	0	< 1	< 20	10	< 0.1
VPOSOUT	5.5	< 25	< 50	5	< 0.1
VNEGOUT	0	< 25	< 50	5	< 0.3
VDETCOM	5.5	< 5	< 5	1	< 10
VCAS [1]	3.75	< 1	< 1	5	< 0.1
VOUTREF [1]	3	< 1	< 1	5	1
VBLM [1]	2	< 1	< 5	50	< 0.1
	Levels (volts)	**Load** (pF)	**Rise/Fall** (nsec)	**Max. Ext. Resistance** (Ω)	
Clocks					
CLK	0-5.5	< 20	< 10	25	
FSYNC	0-5.5	< 10	< 10	25	
LSYNC	0-5.5	< 10	< 10	25	
DATA	0-5.5	< 10	< 10	25	
	Levels (volts)	**Load** $C_{out}//R_{out}$ (pF // kΩ)	**Settle** (to .1%, nsec)	**Max. Ext. Resistance** (Ω)	
Outputs					
OUTA, OUTB, OUTC, OUTD	1.7-4.5	25//500	50	50	
OUTR	3	25//500		50	
Test and Miscellaneous	**Voltage**				
IMSTRADJ [2]	0-5.5			50	
TEMP	0-5.5			50	
GAIN [2]	0-5.5			50	
BWL [2]	0-5.5			50	
VOS	0-5.5			5	
TESTOUT	0-5.0			N.C.	
VTESTIN	1.5-4.5			N.C.	

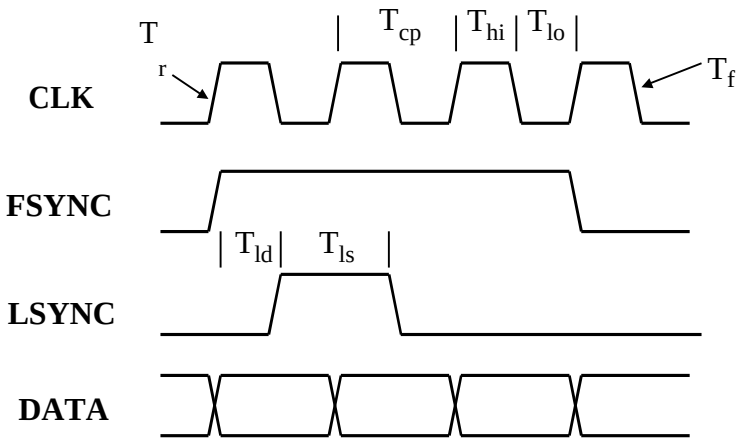
1. Generated internally but can be overridden
2. Also addressable through control register (along with windowing and readout format invert/revert)



ISC9809 Suggested Bias Supply Filtering for Noise Considerations

Switching Specifications Full Temperature Range					
Parameter	**Name**	**Min.**	**Typ.**	**Max.**	**Units**
Trise [1]	Tr		10	20	ns
Tfall [2]	Tf		10	20	ns
Tsetup and hold [3]	Tsh	5			ns
Clock Duty Cycle [4]	Tcp	200			ns
Clock High [5]	Thi		0.5*Tcp		ns
Clock Low [5]	Tlo		0.5 *Tcp		ns
LSYNC width	Tls		1 *Tcp		ns
LSYNC and FSYNC delay	Tld	0.5*Tcp			

NOTES:
1. 10-90% (all signals)
2. 90-10% (all signals)
3. All signals to CLK edge
4. 10MHz pixel rate
5. Clock duty cycle = 50%



4 Pinout Description

Pin #	Signal Name	PINS Description	I/O type
1	**VDETCOM**	**Detector Common:** Detector Supply voltage, adjust detector bias voltage, connected to the detector common hybridization ring	P
2	**VPOS_CORE**	**Analog Supply:** This is the positive supply for the CTIA amplifier	P
3	**TEMP**	**Buffered Temperature Diode:** This pin may be used to read a voltage, referencing the temperature of the chip.	AO
4	**TESTOUT**	**Test Mode Output:** Function is set through the control register	CO
5	**VTESTIN**	**Test Mode Control Signal:** Test input used when no detector is connected	TA
6	**BWL**	**CTIA Amplifier Bandwidth Select:** Also addressable through the Control Command Register	CL
7	**GAIN**	**Integration Capacitor Select:** Also addressable through the Control Command Register	CL
8	**DATA**	**Serial Control Register Data**: This digital input is used to program the Serial Control Register when operating the chip in Command Mode. This input is not connected in Default Mode and is internally pulled down.	CI
9	**FSYNC**	**Frame Synchronization Signal:** This signal is used to synchronize the start of a frame, invoke new commands loaded in the Serial Control Register and control the integration time.	CI
10	**LSYNC**	**Line Synchronization Signal:** Control the line readout timing	CI
11	**CLK**	**Master Clock:** This signal is used to load commands on the DATA input pin into the Serial Control Register. Pixel data is clocked on both the edge of CLK. Data is loaded into the Serial Control Register only on the falling edge of CLK.	CI
12	**VPD**	**Digital Supply:** This is the positive supply for all the digital circuits.	P
13	**VND**	**Digital Return:** Ground node for all the digital circuits.	P
15	**VNEGOUT**	**Output Ground:** Output driver negative supply	P
16	**OUTA**	**Video Output:** Output A – Used in single output mode	VO
17	**OUTB**	**Video Output:** Output A and B used in two outputs mode	VO
18	**OUTC**	**Video Output:** Output A, B, C and D used in four outputs mode	VO
19	**OUTD**	**Video Output:** Output A, B, C and D used in four outputs mode	VO
20	**OUTR**	**Video Output:** Reference for common mode output	VO
21	**VPOSOUT**	**Output Supply:** Output driver positive supply	P

Pin #	Signal Name	PINS Description	I/O type
22	**VOS**	**Skimming Voltage:** Variable offset/skimming control voltage	R
23	**VBLM**	**Anti-Blooming Voltage:** Detector anti-blooming control	R
24	**VOUTREF**	**Output Reference Level:** Generated internally but can be overridden	R
25	**VCAS**	**CTIA Amplifier cascode FET bias:** Generated internally but can be overridden	R
26	**IMSTR_ADJ**	**Power Override:** Generated internally but can be overridden	R
27	**VNEG**	**Analog Supply:** This is the negative supply and substrate for all analog circuits on the chip except the output driver	P
28	**VPOS**	**Analog Supply:** This is the positive supply for all analog circuits on the chip except the output driver	P
29,30, 31,32	**TESTDET (4-1)**	**Test Detector Pads:** These 4 pads provide a means of connecting to the 4 test detectors.	TD
14		**DO NOT CONNECT TO THIS PAD !** Bonding to this pad could permanently damage the performance of the chip. This pads is used for ROIC factory testing only.	

Explanation of I/O Type Symbols:
AO - Analog Output: Low bandwidth analog output.
DI - Digital Input: Low speed digital signal.
CI - Clock Input: High speed digital signal.
CO - Clock Output: High speed digital output.
P - Power Supply: Power supply or power supply return [ground].
R - Reference Voltage: DC voltage reference
TA - Test Analog Input: DC test voltage
TD - Test Detector I/O: Test detector access [used to test detectors after hybridization]
VO - Video Output: High speed video output pin.

5 Theory of Operation

A general description of the ISC9809 operation is given in this section.

5.1 Input Circuit: CTIA

The ISC9809 uses a capacitive transimpedance amplifier (CTIA) input circuit designed to have minimal readout noise. The detector signal is integrated onto the CTIA feedback capacitor. The voltage on the integration capacitor is sampled and multiplexed to the column amplifier, Figure 3. The detector bias voltage is adjusted through the VDETCOM pad. Bipolar bias adjustment is possible allowing biasing of both p-on-n and n-on-p type of detectors.

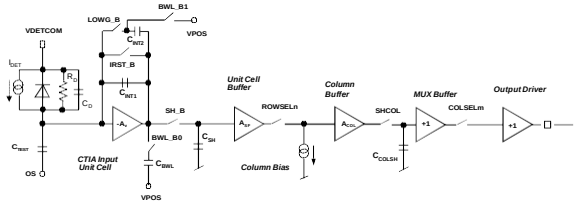


Figure 3: ISC9809 Analog Signal Path

The CTIA has two selectable integration capacitors (10fF and 210fF) allowing $0.17x10^6$ to $3.5x10^6 e^-$ charge capacity, respectively. The gain of the CTIA can be control externally by connecting the GAIN pad low (default) or high (sets 10fF and 210fF respectively). The integration capacitor value can also be set by the Control Register through the GC bit (note: Gain pad must be low or floating to allow GC control).

Integration time is externally adjustable from 5µs (>0.5µs for special ITR mode).

The bandwidth of the amplifier stage can also be controlled for noise optimization. The BWL pad connects or removes one of the bandwidth limiting capacitors on the CTIA amplifier. Bandwidth limiting can also be set by the Control Register through the BW(1-0) bits.

The readout noise floor measured at room temperature, in the default and without detector is less than 70 e^-_{RMS} mode (Cint=10fF) and less than 700 e^-_{RMS} in the low gain mode (Cint=210fF).

Offset adjustment in the signal chain allows skimming of the signal on top of a fixed background or leakage current. The CTIA amplifier has a current skimming function which also enables it to be used with N-on-P detectors such as Pt:Si or HgCdTe under low background conditions (10fF integration capacitor).

A sample-and-hold capacitor is in each unit cell for full frame snap shot integration while reading out the previously integrated frame (IWR).

The unit cell signal is buffered in each cell by a source follower for voltage multiplexing to each column.The column output voltage is buffered, sampled, and multiplexed to high bandwidth output amplifier(s). Voltage mode signal output provides simple interface requirement.

The ISC9809 supports several adjustments optimize power while achieving desired performance for various applications. The default conditions can be overridden in the Command Mode by setting bits in the Serial Control Register, I(2-0) to adjust Master Bias currents for the analog signal path circuits, PWA(1-0) to adjust bias currents for the analog signal path except for the CTIA amplifier bias in the unit cells and AP(2-0) to adjust the CTIA amplifier bias current. For Default Mode operation, the IMSTR_ADJ pad is used to adjust Chip Master Bias currents for the analog signal path circuits. Figure 4 shows the various bias supply adjustments.

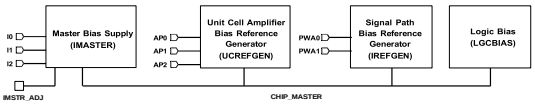


Figure 4: ISC9809 Bias Supply Adjustments

5.2 Output Multiplexer and Buffers

The ISC9809 may be run using from one to four outputs. A common mode reference output can also be enabled. Routing of a given column amplifier to a given output buffer is accomplished through the output multiplexer, shown in Figure 5. The maximum output full frame rate supported in the Default Mode is 110Hz. In the Command Mode, output data rate up to 346 frames per second can be attained. For single output mode, all pixels are readout through OutA. When using multiple outputs, pixels are assigned to a specific output channel, and will be read out through only that channel, regardless of the invert/revert, windowing, and/or line repeat modes selected.

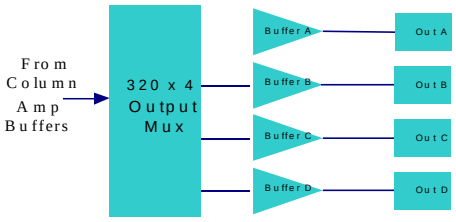


Figure 5: Multiplexing mode

5.3 Integration Modes

The ISC9809 features snapshot mode integration, where all channels integrate simultaneously. The integration time is controlled by the FSYNC pulse. Integrate-While-Read (IWR) and Integrate-Then-Read (ITR) modes of operation are selected by the falling edge of the FSYNC signal.

Integrate-While-Read allows the highest line rates, overlapping the integration of one frame with the readout of the previous frame. The Integrate-Then-Read mode allows the integration to be separated in time from the readout sequence. ITR has lower line rate compared to IWR

A timing pattern for the IWR operation is shown in Figure 6. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. The frame time is approximately equal to the pixel readout time. The integration time occurs during the readout time, allowing for the greatest possible frame rate and integration time duty cycle (where integration time duty cycle = T_{Int} / T_{Frame}).

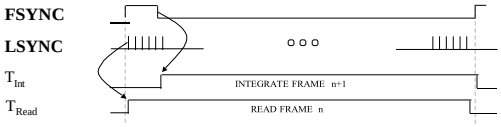


Figure 6: Integrate-While-Read timing T_{Frame}= T_{Read}

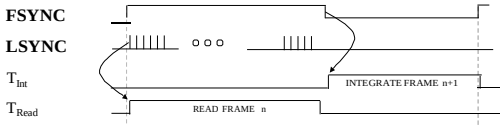


Figure 7: Integrate-Then-Read timing T_{Frame}~T_{read}+T_{Int}

Figure 7 shows a timing pattern for in the ITR mode. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. The integration starts at the falling edge of FSYNC. The frame time is approximately equal to the readout time, resulting in a lower maximum frame rate and integration time duty cycle.

5.4 Temperature Sensor

The ISC9809 has a built-in temperature sensor which is a buffered PN junction potential, Figure 8. The predicted output function of the temperature is shown in Figure 9. The voltage potential at room temperature is ≈0.75V and varies slightly on each device. This is not a calibrated temperature diode but is designed for monitoring the temperature of the device.

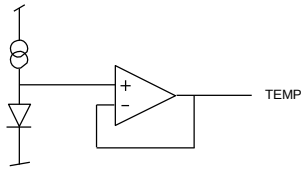


Figure 8: On-chip temperature sensor

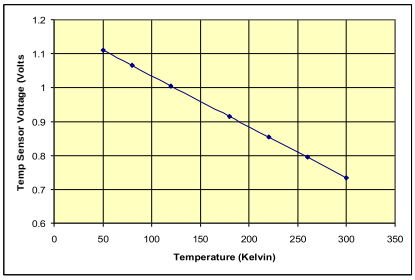


Figure 9: Temperature sensor predicted output voltage Vs temperature

6 Modes of Operation

The ISC9809 has two operation modes, the simplified Default Mode and the programmable Command Mode, which utilizes the advanced features of the ROIC.

6.1 Command Mode

The block diagram for the command mode operation is shown in Figure 10. Command Mode operation utilizes the on-chip Serial Control Register to control device modes and advanced readout features. The fields of the Serial Control Register are illustrated in Figure 11.

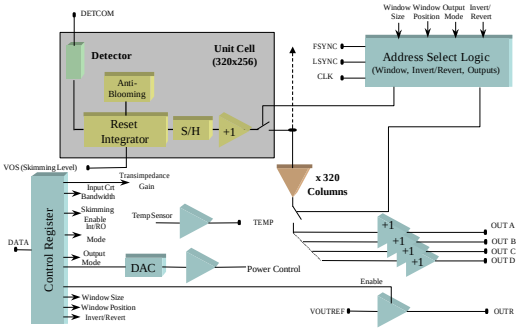


Figure 10: ISC9809 Command Mode Block Diagram

To operate in this mode, the DATA pad must be used to load control words into the Serial Control Register. The settings in the Command Register controls the following functions:

- Window size and location
- Readout direction
- C_{INT} select
- CTIA bandwidth select
- Power control
- Test modes
- 1,2,or 4 output modes
- Reference output enable
- Global reset
- Skimming enable
- Special ITR mode
- Integration/readout modes
- Master reset

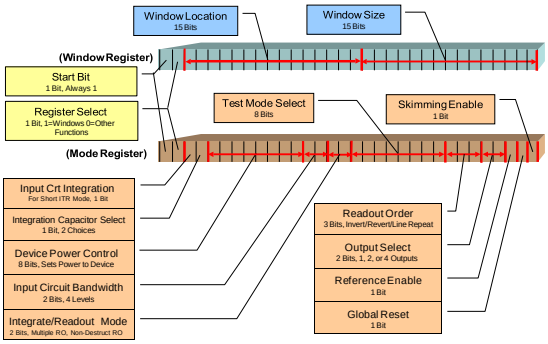


Figure 11: Serial Control Register Fields

6.2 Default Mode

This mode provides a simple interface, with reduced external electronics and power dissipation, for applications where advanced ROIC features or high-speed performance are not required. The Default Mode does not use the on chip Serial Control Register.

In Default Mode the ISC9809 operates with the following configuration:

- GC=0: integration capacitor = 10fF
- OE_EN=0: skimming disable
- ITR=0: normal integration timing
- PW(1-0)=10: mid current
- I(2-0)=100: mid current
- AP(2-0)=100: mid current
- BW(1-0)=00: highest bandwidth
- IMRO=0: normal operation
- NDRO=0: normal operation
- TS(7-0)=00000000: normal operation
- RO(2-0)=000: normal mode (no invert, no revert, no line repeat)
- OM(1-0)=00: single output mode
- RE=0: reference output disable
- WAX(7-0)=00000000: address 0
- WAY(6-0)=0000000: address 0
- WSX(7-0)=00000000: full window
- WSX(6-0)=0000000: full window

The default values occur after a power-on reset or after a master reset command (RST=1).

7 Output Modes

The ISC9809 can be configured to support one, two, four outputs with or without an output reference. In order to invoke any output mode other than single output, with no reference output, the device must be operated in Command Mode. For single output mode, all pixels are read out through OutA. When using multiple outputs, pixels are assigned to a specific output channel, and will be read out through only that channel, regardless of the image transposition (invert/revert), and windowing modes selected.

The lowest left-hand pixel is defined as pixel (0,0), where this annotation signifies the pixel at location row 0, column 0 of the ISC9809 device. Pixel (0,0) is the first pixel to be read out in using default settings for the invert/revert, windowing, and line repeat features. This mode of operation is chosen for a normal 'inverting optic'. Given this type of optic, a 'normal' raster scan image will be presented by placing the bottom row (row 0) at the 'bottom' of a camera system.

When two outputs are selected, the first pixel is presented at OutA, and the second pixel is presented at OutB. Alternate pixels are presented at the A and

B output channels, respectively. When four outputs are selected, the first pixel is presented at OutA, the second pixel is presented at OutB, the third pixel at OutC, and the fourth at OutD.
Alternating in four pixel increments, pixels are presented at the A, B, C and D output channels, respectively. Figure 12 shows the assigned channels and readout order for four outputs and the various modes.
Figure 13 gives the minimum window sizes in the various output modes of operation.

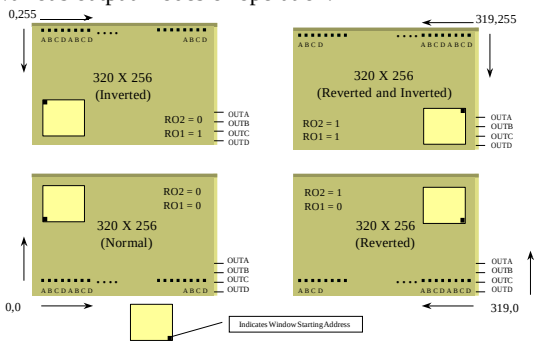
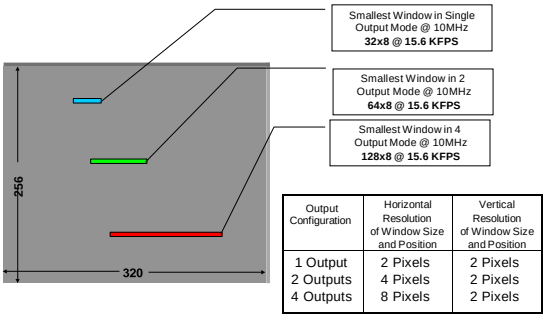


Figure 12: Four Output Mode Readout Order



Output Configuration	Horizontal Resolution of Window Size and Position	Vertical Resolution of Window Size and Position
1 Output	2 Pixels	2 Pixels
2 Outputs	4 Pixels	2 Pixels
4 Outputs	8 Pixels	2 Pixels

Figure 13. Windowing Operation

8 Physical Characteristics

The ISC9809 is built using a standard 0.6µm CMOS process with triple metal and double polysilicon layers. The die size is 11.35mm by 10.65mm as measured to the edge of the scribe lane. The die are processed on 5 inch (125mm) wafers which have a thickness of 625µm +/- 25µm. There are 72 per wafer with a 200µm scribe lane in both the x and y directions.

WARNING ! Electrostatic Discharge Sensitive Device
Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment. This can discharge with out detection and cause permanent damage. The ISC9705 features proprietary ESD protection circuitry, however permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss or functionality.